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fides et ratio

Two Dimensional Supersonic Flow Simulation on Array Computers

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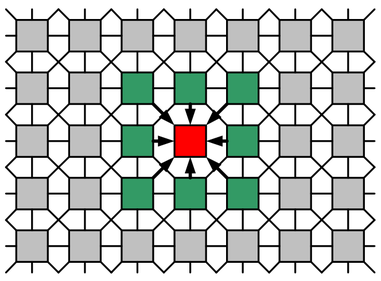
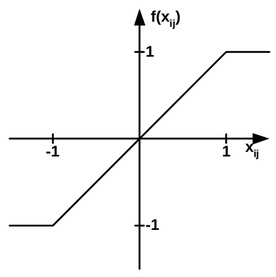
Cellular Neural Networks (CNN)

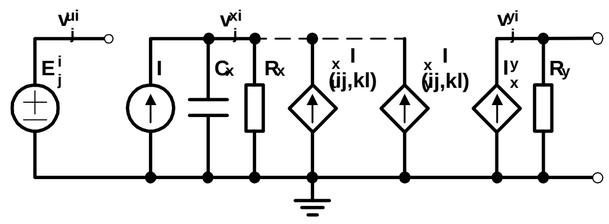
Locally connected analog processors



Output nonlinearity



Electrical model of one analog processor

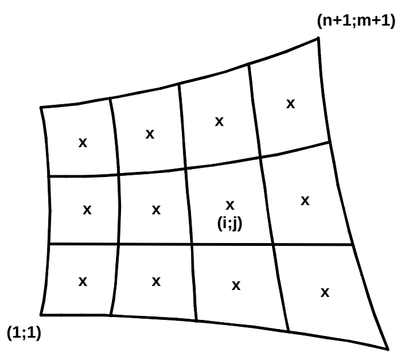


State equation of one analog processor

$$C_x \dot{v}_{xij}(t) = -\frac{1}{R_x} v_{xij}(t) + \sum_{kl \in S_r(ij)} A_{ij,kl} \cdot v_{ykl}(t) + \sum_{kl \in S_r(ij)} B_{ij,kl} \cdot v_{ukl}(t) + z_{ij}$$

Euler equations

Derived from the Navier-Stokes Equations
Describes the dynamics of
- dissipation-free
- inviscid
- compressible fluids



$$\frac{\partial \rho}{\partial t} + \nabla \cdot (\rho \mathbf{v}) = 0$$ **Continuity Equation**

$$\frac{\partial (\rho \mathbf{v})}{\partial t} + \nabla \cdot (\rho \mathbf{v}\mathbf{v} + \hat{I}p) = 0$$ **Momentum Equations**

$$\frac{\partial E}{\partial t} + \nabla \cdot ((E + p)\mathbf{v}) = 0$$ **Energy Equation**

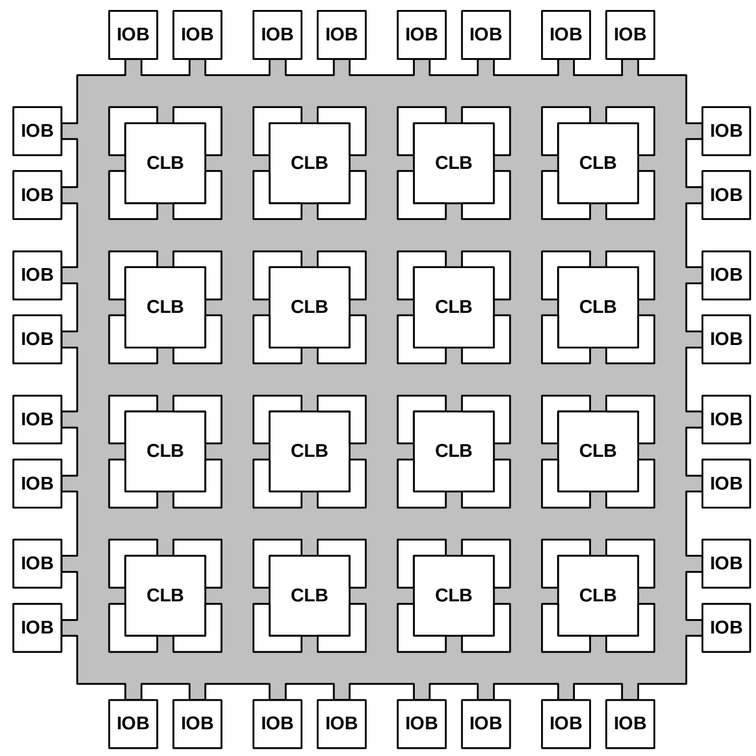
Spatial discretization on a body fitted mesh
Temporal discretization (Lax-Friedrichs)
Logically structured data arrangement
Solution on array processors is motivated by Cellular Neural Network

Field Programmable Gate Array (FPGA)

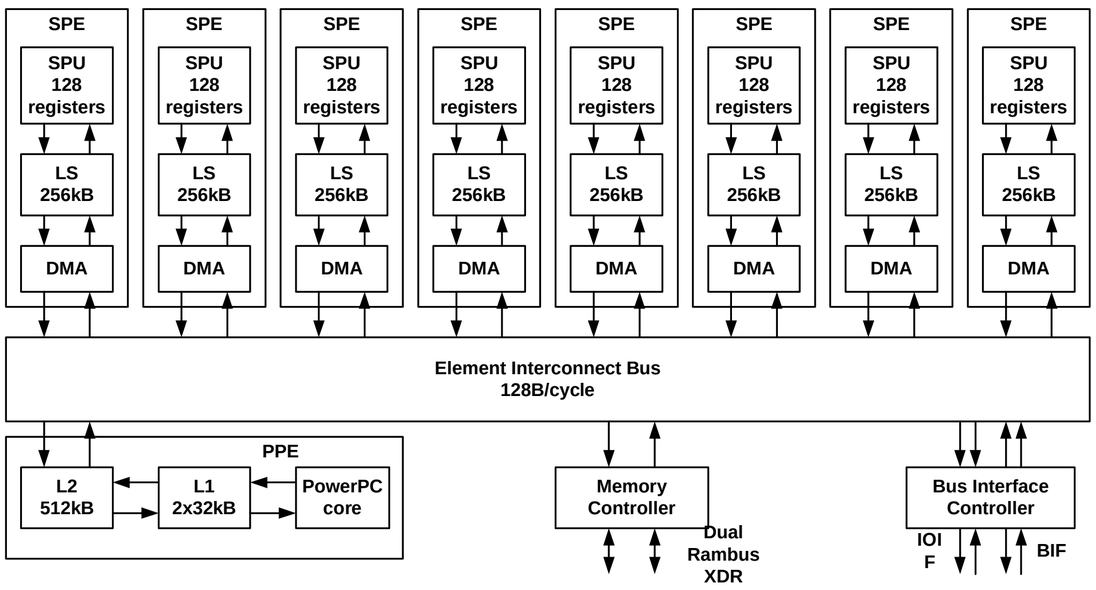
Xilinx Virtex-5 FPGA
- 37,440 Configurable Logic Blocks (CLB)
- 1056 25x18bit Multipliers
- 11Mbit on-chip RAM
- PCI-Express Endpoint
- Gigabit Ethernet MAC

Performance
- 580GMACS (25bit integer)
- 190GFLOPS (Single-precision)
- 65GFLOPS (Double-precision)

FPGA Architecture



IBM Cell Broadband Engine Architecture



Multiprocessor on a chip
- 241M transistors, 235mm2
- 230.4GFlops (Single-precision)
- 102.4GFlops (Double-precision)

1 Power Processor Element (PPE)
- general purpose
- running full-fledged OSs

8 Synergistic Processor Element (SPE)
- optimized for compute density

IBM BladeCenter System
QS22 Cell Blade
- Dual IBM PowerXCell 8i processor
- 16GB DDR2 SDRAM
- 4x DDR Infiniband

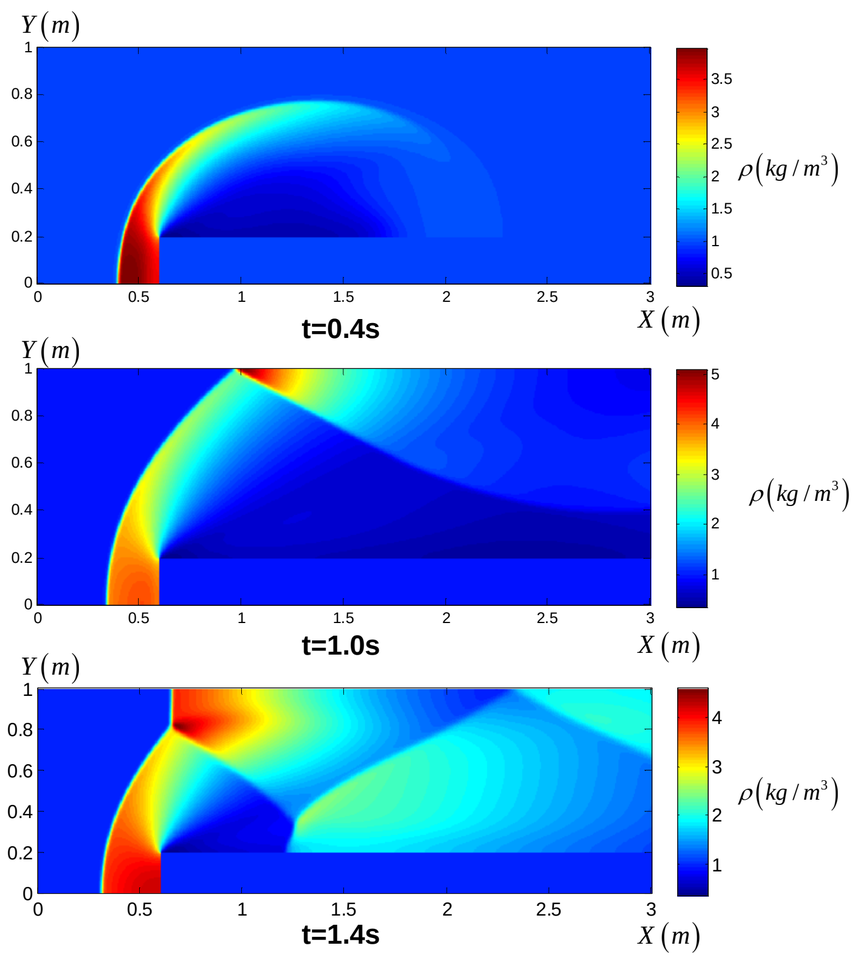
up to 14 Blades per Chasis
- 6.451TFlops/Chasis (Single-precision)
- 2.867TFlops/Chasis (Double-precision)

Implementation on IBM Cell and Xilinx Virtex-5 FPGA

IBM Cell	Xilinx Virtex-5 FPGA
- Multi-threaded implementation	- Specialized re-configurable hardware accelerator
- SPE optimized algorithm	- High Level Hardware Description
- Relatively short development time	- Longer development time
- Performance improvement *	- Performance improvement *
- 34 times using 1 SPE (Single-precision floating-point)	- 688 times using Single-precision floating-point numbers
- 240 times using 8 SPEs (Single-precision floating-point)	- 494 times using Double-precision floating-point numbers
	- 3075 times using 32bit fixed-point numbers

*Compared to an Intel Core2Duo T7200 microprocessor

Simulation of a Mach3 Flow Over a Forward Facing Step



Additional details: S. Kocsárdi, Z. Nagy, Á. Csík, P. Szolgay "Two-dimensional Compressible Flow Simulation on Emulated Digital CNN-UM", Internat ional Journal of Circuit Theory and Applications, Vol. 37, Issue 4, pp. 569-585, 2009, DOI: 10.1002/cta.565