A TUDOMÁNYOS KUTATÁSOK KIBONTAKOZTATÁSA
A PÁZMÁNY PÉTER KATOLIKUS EGYETEMEN
TÁMOP-4.2.1.B-11/2/KMR-2011-0002

NEW SZÉCHENYI PLAN

Pázmány Péter Catholic Univesity

Array and multi-processor architectures

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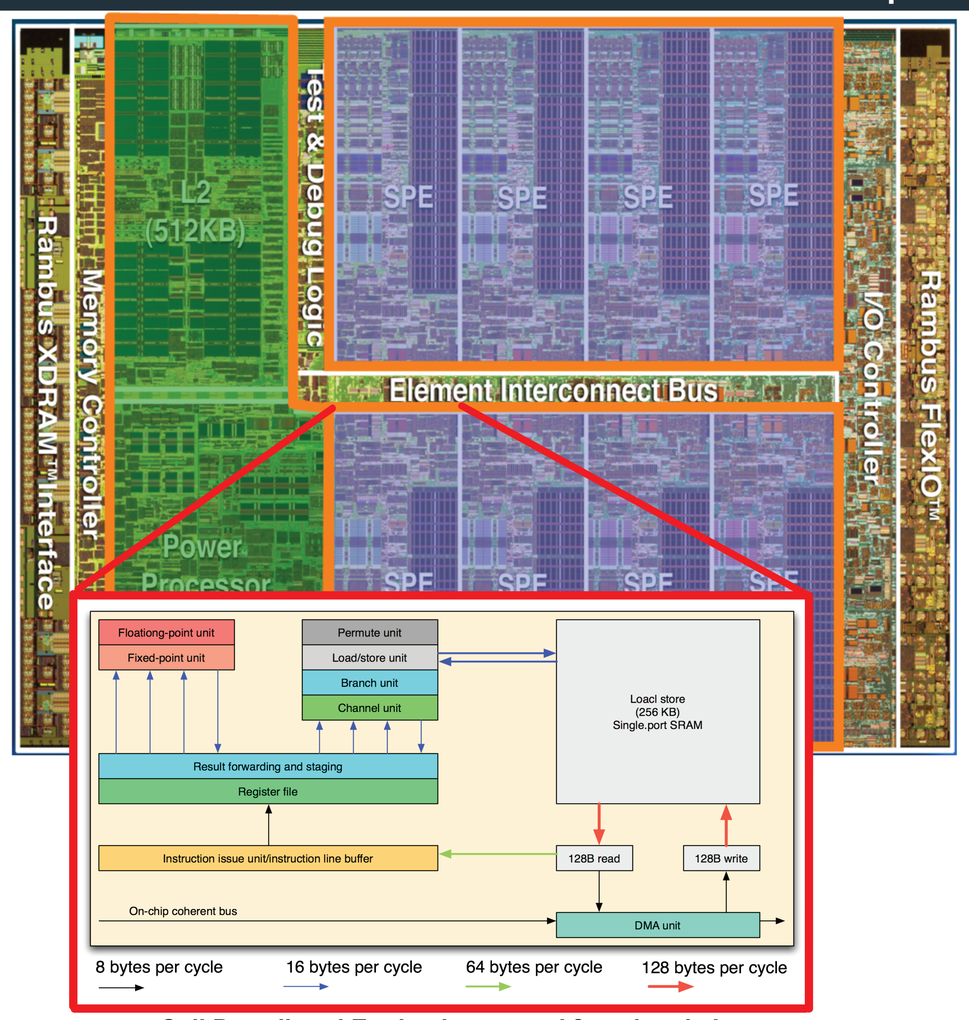
Cell multi-processor



Cell Broadband Engine layout and functional elements

- Sony
- IBM
- Toshiba

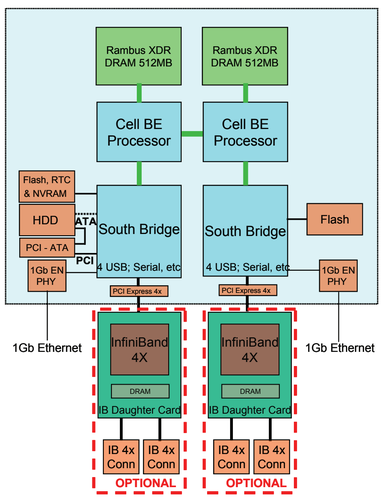
- Multiprocessor on a chip
  - 241M transistors, 235mm^2
  - 200 GFlops (SP) @3.2GHz
  - 200 GB/s bus (internal) @ 3.2GHz
- Power Processor Element (PPE)
  - general purpose
  - running full-fledged OSs
- Synergistic Processor Element (SPE)
  - optimized for compute density

- Heterogeneous, multi-core engine
  - 1 multi-threaded power processor
  - up to 8 compute-intensive-ISA engines
- Local Memories
  - fast access to 256KB local memories
  - globally coherent DMA to transfer data
- Pervasive SIMD
  - PPE has VMX
  - SPEs are SIMD-only engines
- High bandwidth
  - fast internal bus (200GB/s)
  - dual XDR™ controller (25.6GB/s)
  - two configurable interfaces (76.8GB/s)
  - numbers based on 3.2GHz clock rate

Playstation with Cell multi-processor

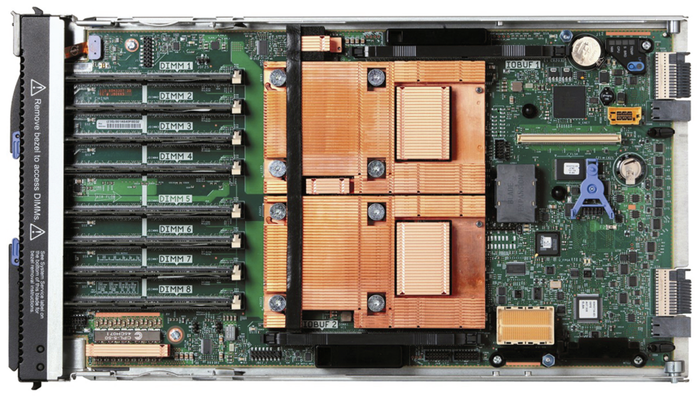
IBM BladeCenter

- Cell BE Processor Blade **(~500GFLOPS peak)**
  - Dual 3.2GHz Cell BE Processor Configuration
  - 1GB XDRAM (512MB per processor)
  - Blade-mounted 40GB IDE HDD
  - Dual Gigabit Ethernet (GbE) controllers
  - Double-wide blade (uses 2 BladeCenter slots)
  - Infiniband (IB) Option:
    - Qty 0-2 IB 4x Host Channel Adapters
- BC Chassis Configuration **(~3.5TFLOPS peak)**
  - Standard IBM BladeCenter One
  - Max. 7 Blades per chassis (QS20 - 2 slots each)
  - 2 Gigabit Ethernet switches
  - External IB switches required for IB option



Cell Blade architecture

IBM BladeCenter H



IBM/Cell QS

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HUNGARY'S RENEWAL

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